METHOD FOR TESTING MEMORIES WITH SEAMLESS DATA INPUT/OUTPUT BY INTERLEAVING SEAMLESS BANK COMMANDS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for testing memories, and more particularly to a method for testing memories with seamless data input/output by interleaving seamless bank commands so as to detect a weakened memory.

2. Description of Related Art

While dynamic random access memories (DRAM) are manufactured by 0.2 μm process technology or an advanced manufacturing process, a power supply is lower than 3.3 volts, and a clock rate applied is higher than 133 megahertz, and the DRAM performance is then more and more sensitive to noise from external command signals, address signals, input data signals, and intrinsic noise raised from internal circuitry. For such consideration, DRAM designers have to carefully design memory circuits to provide correct data storage/access paths from each memory cell. On the other hand, DRAM manufacturing engineers must carefully control process conditions to guarantee target device/circuit performance. Even so, weakened memory cells still sometimes exist in DRAM chips and weakened data are probably stored. Thus, a challenge to test engineers is to provide a testing program to screen those memories and assist circuit designers to find critical data access paths and to cover device weakness.

A memory testing program is assembled by a pin condition setting, and a data access pattern. The pin condition setting includes setting of commanding pins, addressing pins and I/O pins. The data access pattern is used to define word-by-word data access paths and its corresponding operational clock rate. The pin condition setting, which includes true table setting and logic high/low voltage setting, is based on DRAM specification reference to data sheet. The data access pattern is, on the other hand, created by specific testing purposes. For instance, a one-dimensional row access pattern for accessing memory cells on a fixed word line (W/L) is applied to check word line continuity; and a one-dimensional column access pattern for accessing memory cells located on the same column is applied to check bit line (B/L) continuity. In the book "Testing Semiconductor Memory" written by A.J. van de Goor, published by John Wiley & Sons, there are traditional two-dimensional checkboards, GALPAT, sliding diagonals, butterfly patterns etc. for providing better fault coverage.

Usually, programming commands loops are used to carry out the access patterns mentioned above. For example, a memory has four banks (#0~#3) are shown in Figs. 5, 6A and 6B, a programmable cycling control command "Bank active - Write or Read - Bank pre-charge" is applied in the single bank (Bank #0), wherein the burst length in Figs. 5, 6A and 6B is 4. In Fig. 5, while a "write" command is generated, data having four clock lengths are outputted from data input/output terminals (DQ). In Figs. 6A and 6B, while a "read" command is generated, data in DQ respectively has two and three clock latency. This kind of cycling command is generally used to check

basic functions of DRAM chips, however data in DQ are not inputted/outputted seamlessly.

With reference to Figs.7, 8A and 8B, those figures are similar to Figs. 5, 6A and 6B, with a difference being that a programmable cycling command "Bank active - Write with auto pre-charge or Read with auto pre-charge" is applied in a single bank (Bank #0). This kind of loop is used to check functions of an auto pre-charge.

With reference to Figs. 9 to 12, those figures disclose an interleave bank operation. Two banks interleave and four banks interleave operations are shown in Figs. 9~10 and Figs. 11~12 respectively. Such repeated operations are capable to do seamless input/output (I/O) checks for examining I/O performance. Clearly, the operations shown in Figs. 9 to 12 suffer larger noise due to more compact I/O operations than those shown in Figs. 5 to 8. Although DQ in Figs. 9 to 12 are inputted/outputted data seamlessly, control pins of memory still do not receive seamless controlling commands. Even four banks (Bank #0, #1, #2 and #3) receive initial "active" commands, the control pins still retain in a "wait" situation at 14th, 15th, 18th, 19th, 22nd, 23rd, 26th, 27th, clock cycles. Thus the commands shown in Figs. 9 to 12are not sufficient to detect weakened memory cells.

To overcome these shortcomings, the present invention tends to provide a method for testing a memory with seamless data input/output by interleaving seamless bank commands to mitigate and obviate the aforementioned problems.

SUMMARY OF THE INVENTION

The main object of the present invention is to provide a method for testing memories with seamless data input/output by interleaving seamless bank commands so as to provide seamless data and commands to data input/output pins and control pins of the memory.

The second object of the present invention is not only to provide a method that suits testing SDRAMs, but also suits testing DDR DRAMs and RDRAMs.

To achieve the main object, the method in accordance with the present invention comprising steps of :

transferring data to data input/output (I/O) pins of memories seamlessly;

inputting control commands to control pins of the memories seamlessly.

Thus control pins and data input/output pins of memories receive heavy loading due to the seamless control commands, whereby the weakened memories are easily to detect.

Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C respectively show a memory testing timing sequence view of first to third embodiments in accordance with the present invention;

Figs. 2A to 2D respectively show a memory testing timing sequence view of fourth to seventh embodiments in accordance with the present

invention;

Figs. 3A to 3C respectively show a DDR-DRAM memory testing timing sequence view in accordance with the present invention;

Figs. 4A and 4B respectively show a RDRAM memory testing timing sequence view in accordance with the present invention;

Fig. 5 is a timing sequence view of a conventional memory testing method showing data writing in a single bank;

Figs. 6A and 6B are timing sequence views of a conventional memory testing method showing data reading in a single bank;

Fig. 7 is a timing sequence view of a conventional memory testing method showing data writing and auto pre-charge in a single bank;

Figs. 8A and 8B are timing sequence views of a conventional memory testing method showing data reading and auto pre-charge in a single bank; and

Figs. 9, 10A, 10B, 11, 12A and 12B are timing sequence views of a conventional memory testing method showing data reading/writing in multi-banks。

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is a method for testing a memory by providing seamless control commands and data, wherein the memory has at least two banks. By providing seamless control commands and data, the control pins and data input/output pins of the memory receive heavy loading due to the seamless control commands. For SDRAMs and DDR-DRAMs, control commands and data are seamlessly inputted/outputted at each clock cycle.

For RDRAMs, control commands are inputted at each "command packet", whereby data are inputted/outputted at each "data packet" and memories are in heavy loading status. By providing heavy loading to memories, it is easy to detect weakened memories.

In the following description, "DQ" that appears in figures in accordance with the present invention is used to represent data input/output terminals.

With reference to Figs. 1A, 1B and 1C, timing sequence views respectively having burst lengths of 2, 4 and 8 with different cycling control commands are shown.

With reference to Fig. 1A, after banks #0 ~ #3 serially receive "active" commands with two clock cycle intervals, control commands "write with auto pre-charge" are inputted to each bank at appropriate intervals. Thus after the bank #3 receives the initial "active" command, control commands (including "active" and "write with auto-pre charge") are sequentially inputted to the banks #0~#3 at each clock cycle, whereby data input/output terminals (DQ) have seamless data input/output and remains in a heavy loading status.

With reference to Fig. 1B, the burst length is 4 and the cycling control commands are programmed as "active, write, write, bank pre-charge", and the data input/output terminals (DQ) still haveseamless data input/output.

With reference to Fig. 1C, the burst length is 8. Different types of cycling control commands are provided to each bank. In the bank #0, the control commands are "active, write, write, bank pre-charge, active, bank

pre-charge, active, bank precharge". In the bank #1, the control commands are "active, bank pre-charge, active, write, write, bank pre-charge, active". In the bank #2, the control commands are "active, bank pre-charge, active, bank pre-charge, active, write, write". In the bank #3, the control commands is another type that differs from the control commands in banks #0 ~ #2. Although the control commands types for each bank are different, control pins and data input/output terminal (DQ) still remain in a heavy loading status.

With reference to Figs. 2A and 2B, cycling control commands "active, bank with auto pre-charge" are applied to each bank with different latencies(2 and 3). At each clock cycle, one of the banks (bank #0 ~ #3) still receives a control command, and the data input/output terminals (DQ) has seamless data input/output.

The present invention not only provides seamless data and control commands to data input/output terminals (DQ) and control pins, but also depends on memory testing requirement to provide a purposeful interrupt or delay to control commands.

With reference to Fig. 2C, a control command "CKE" is inserted in the cycling control commands, thus the next control command has a one clock cycle delay, whereby the operating accuracy of memories is easily detected.

With reference to Fig. 2D, a mask control command "DQM" is inserted in the cycling control commands at a purposeful clock cycle, thus data at the purposeful clock cycle are masked.

The present invention also suits application for DDR-DRAMs and

RDRAMs.

With reference to Figs. 3A, 3B and 3D, timing sequence views of testing DDR-DRAMs with data writing/reading are respectively shown. The cycling control commands of DDR-DRAMs are similar to the control commands mentioned above. The difference between the data inputting/outputting status of Figs. 3A, B and D, and the data inputting/outputting status mentioned above is that two data appear at the same clock cycle.

With reference to Figs. 4A, 4B and 4C, timing sequence views of testing RDRAMs with data writing/reading are respectively shown, wherein control commands and data are inputted/outputted seamlessly at each "packet" not "clock cycle".

Although the present invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.